

## CLAIMS

What is claimed is:

- 5     1.     A data storage system, comprising:
- power circuitry configured to provide power signals;
- storage processing circuitry configured to perform data storage operations;
- and
- a packaged microcontroller coupled to the power circuitry and the storage
- 10       processing circuitry, the packaged microcontroller having a set of input lines, a set
- of output lines, and control circuitry coupled to the set of input lines and the set of
- output lines, the control circuitry being configured to:
- receive, on the set of input lines, a first set of power signals
- which is provided by the power circuitry to the storage processing
- 15       circuitry,
- wait a predetermined time period in response to receipt of
- the first set of power signals on the set of input lines, and
- output, through the set of output lines, a set of enable
- signals to the power circuitry after waiting the predetermined time
- 20       period, the set of enable signals directing the power circuitry to
- provide a second set of power signals to the storage processing
- circuitry.

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2. The data storage system of claim 1 wherein the packaged microcontroller further includes:

a set of built-in analog-to-digital converters coupled to the set of input lines and to the control circuitry, the control circuitry being configured to compare a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry.

3. The data storage system of claim 2 wherein the packaged microcontroller further includes:

memory which stores pre-loaded code having a version identifier, the control circuitry being configured to:

compare the version identifier of the pre-loaded code with a version identifier of available new code, and

replace the pre-loaded code stored in the memory with the available new code when the version identifier of the available new code indicates that the available new code is newer than the pre-loaded code, and maintain the pre-loaded code within the memory when the version identifier of the available new code indicates that the available new code is not newer than the pre-loaded code.

4. The data storage system of claim 3 wherein the packaged microcontroller further includes:

a dedicated memory location, wherein the control circuitry, when replacing the pre-loaded code stored in the memory with the available new code, is

5 configured to:

set the dedicated memory location with a flag to indicate that a code replacement routine is in progress,

overwrite the pre-loaded code stored in the memory with the available new code, and

10 clear the dedicated memory location to remove the flag to indicate that no code replacement routine is in progress.

5. The data storage system of claim 2, further comprising:

a power button,

15 wherein the packaged microcontroller further includes a persistent memory, the control circuitry being configured to:

access the persistent memory to determine whether the power button of has been toggled to an "ON" position or an "OFF" position, and

20 place the storage processing circuitry in one of (i) a normal operating state when the persistent memory indicates that the power button has been toggled to the "ON" position, and (ii) a recovery state when the persistent memory indicates that the power button has been toggled to the "OFF" position.

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6. A packaged microcontroller for controlling a data storage system having (i) power circuitry for providing power signals and (ii) storage processing circuitry for performing data storage operations, the packaged microcontroller comprising:

a set of input lines;

5 a set of output lines; and

control circuitry coupled to the set of input lines and the set of output lines, the control circuitry being configured to:

10 receive, on the set of input lines, a first set of power signals which is provided by the power circuitry to the storage processing circuitry,

wait a predetermined time period in response to receipt of the first set of power signals on the set of input lines; and

15 output, through the set of output lines, a set of enable signals to the power circuitry after waiting the predetermined time period, the set of enable signals directing the power circuitry to provide a second set of power signals to the storage processing circuitry.

7. The packaged microcontroller of claim 6, further comprising:

20 a set of built-in analog-to-digital converters coupled to the set of input lines and to the control circuitry, the control circuitry being configured to compare a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the  
25 storage processing circuitry.

8. The packaged microcontroller of claim 7, further comprising:  
memory which stores pre-loaded code having a version identifier, the  
control circuitry being configured to:  
compare the version identifier of the pre-loaded code with a  
5 version identifier of available new code; and  
replace the pre-loaded code stored in the memory with the  
available new code when the version identifier of the available new  
code indicates that the available new code is newer than the pre-  
loaded code, and maintain the pre-loaded code within the memory  
10 when the version identifier of the available new code indicates that  
the available new code is not newer than the pre-loaded code.
9. The packaged microcontroller of claim 8, further comprising:  
a dedicated memory location, wherein the control circuitry, when replacing  
15 the pre-loaded code stored in the memory with the available new code, is  
configured to:  
set the dedicated memory location with a flag to indicate  
that a code replacement routine is in progress,  
overwrite the pre-loaded code stored in the memory with  
20 the available new code, and  
clear the dedicated memory location to remove the flag to  
indicate that no code replacement routine is in progress.
10. The packaged microcontroller of claim 7, further comprising:  
25 a dedicated memory location; and  
memory having a main portion which stores pre-loaded main code and a  
secondary portion which stores pre-loaded secondary code, wherein the control  
circuitry is further configured to:

access the dedicated memory location to determine whether a flag is set to indicated that a code replacement routine is in progress, and

5                   run (i) the pre-loaded main code stored in the main portion of the memory when the dedicated memory location is not set with the flag, and (ii) the secondary code stored in the secondary portion of the memory when the dedicated memory location is set with the flag.

10    11.    The packaged microcontroller of claim 7 wherein the data storage system has a power button, and wherein the packaged microcontroller further comprises:

                  a persistent memory, the control circuitry being configured to:

                                  access the persistent memory to determine whether the power button of has been toggled to an "ON" position or an "OFF" position, and

15                               place the storage processing circuitry in one of (i) a normal operating state when the persistent memory indicates that the power button has been toggled to the "ON" position, and (ii) a recovery state when the persistent  
20                               memory indicates that the power button has been toggled to the "OFF" position.

12.    The packaged microcontroller of claim 11 wherein the control circuitry is further configured to:

25                   prior to placing the storage processing circuit in one of the normal operating state and the recovery state, communicate with another packaged microcontroller to determine whether other storage processing circuitry of the data storage system is entering a normal operating state or a recovery state.

13. A packaged microcontroller for controlling a data storage system having (i) power circuitry for providing power signals and (ii) storage processing circuitry for performing data storage operations, the packaged microcontroller comprising:
- 5                   a set of input lines;
- a set of output lines; and
- control circuitry coupled to the set of input lines and the set of output lines, the control circuitry including:
- means for receiving, on the set of input lines, a first set of
- 10                   power signals which is provided by the power circuitry to the storage processing circuitry,
- means for waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines;
- and
- 15                   means for outputting, through the set of output lines, a set of enable signals to the power circuitry after waiting the predetermined time period, the set of enable signals directing the power circuitry to provide a second set of power signals to the storage processing circuitry.
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14. In a packaged microcontroller, a method for controlling a data storage system having (i) power circuitry for providing power signals and (ii) storage processing circuitry for performing data storage operations, the method comprising:
- receiving, on a set of input lines of the packaged microcontroller, a first set
- 25                   of power signals which is provided by the power circuitry to the storage processing circuitry;
- waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines; and

outputting, on a set of output lines of the packaged microcontroller, a set of enable signals to the power circuitry after waiting the predetermined time period, the set of enable signals directing the power circuitry to provide a second set of power signals to the storage processing circuitry.

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15. The method of claim 14 wherein the packaged microcontroller further includes a set of built-in analog-to-digital converters coupled to the set of input lines, and wherein receiving the first set of power signals includes:

10 comparing a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry.

- 15 16. The method of claim 15 wherein the packaged microcontroller includes memory which stores pre-loaded code having a version identifier, and wherein the method further comprises:

comparing the version identifier of the pre-loaded code with a version identifier of available new code; and

20 replacing the pre-loaded code stored in the memory with the available new code when the version identifier of the available new code indicates that the available new code is newer than the pre-loaded code, and maintaining the pre-loaded code within the memory when the version identifier of the available new code indicates that the available new code is not newer than the pre-loaded code.

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17. The method of claim 16 wherein replacing the pre-loaded code stored in the memory with the available new code includes:
- setting a dedicated memory location with a flag to indicate that a code replacement routine is in progress;
  - 5       overwriting the pre-loaded code stored in the memory with the available new code; and
  - clearing the dedicated memory location to remove the flag to indicate that no code replacement routine is in progress.
- 10   18. The method of claim 15 wherein the microcontroller includes memory having a main portion which stores pre-loaded main code and a secondary portion which stores pre-loaded secondary code, and wherein the method further comprises:
- accessing a dedicated memory location to determine whether a flag is set to indicated that a code replacement routine is in progress; and
  - 15       running (i) the pre-loaded main code stored in the main portion of the memory when the dedicated memory location is not set with the flag, and (ii) the secondary code stored in the secondary portion of the memory when the dedicated memory location is set with the flag.
- 20   19. The method of claim 15 wherein the data storage system has a power button, and wherein the method further comprises:
- accessing a persistent memory to determine whether the power button of has been toggled to an "ON" position or an "OFF" position; and
  - 25       placing the storage processing circuitry in one of (i) a normal operating state when the persistent memory indicates that the power button has been toggled to the "ON" position, and (ii) a recovery state when the persistent memory indicates that the power button has been toggled to the "OFF" position.

20. The method of claim 19, further comprises:
- prior to placing the storage processing circuit in one of the normal  
operating state and the recovery state, communicating with another packaged  
microcontroller to determine whether other storage processing circuitry of the data  
5 storage system is entering a normal operating state or a recovery state.